**Finite State Machine**

Q1. The state table of a finite-state machine (FSM) with one input and 2 outputs and is given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Present State | Next State | | Output | |
|  |  |  |  |
| S0 | S2 | S1 | 0 | 0 |
| S1 | S2 | S1 | 0 | 1 |
| S2 | S2 | S3 | 1 | 0 |
| S3 | S1 | S3 | 0 | 0 |

1. Explain weather the given FSM is a Moore-type or Mealy-type state machine?
2. The given FSM is to be implemented as a synchronous sequential circuit with T flip-flops using the state assignments: S0=00, S1=01, S2=10, S3=11. Derive the equations for the inputs to the T flip-flops, and the equations for the outputs and

Q2. The state diagram for a finite state machine (FSM) with one input w and two outputs z2 and z1 is given below:

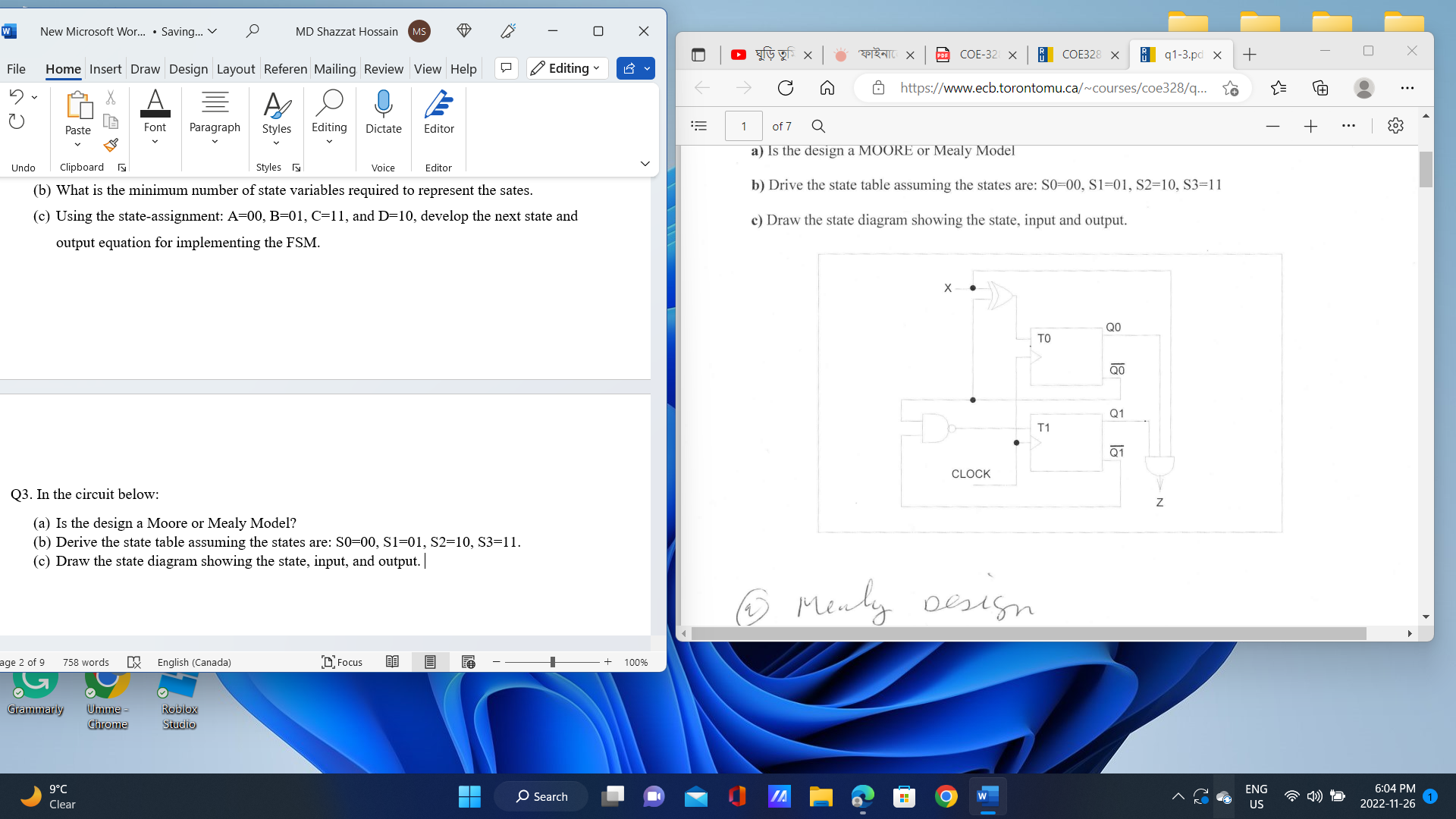
Graphical user interface, application, Word

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1. Does the above state diagram use a Moore or Mealy-type model to represent the FSM? Explain your answer.
2. What is the minimum number of state variables required to represent the sates.
3. Using the state-assignment: A=00, B=01, C=11, and D=10, develop the next state and output equation for implementing the FSM.

Q3. In the circuit below:

1. Is the design a Moore or Mealy Model?
2. Derive the state table assuming the states are: S0=00, S1=01, S2=10, S3=11.
3. Draw the state diagram showing the state, input, and output.



Q4. Consider the following circuit which implements a finite-state machine (FSM):

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1. Derive the state assigned table for the FSM.
2. Complete the following timing diagram for the circuit by assuming Q1=Q0=0 at the beginning.
3. Derive the state assigned table if JK flip-flops (instead of D flip-flops) are to be used to implement the FSM.

Q5. Given the following logic circuit, derive its state table and state diagram. If the following sequence 1010110101 is applied to the x input of the circuit with initial state 01, determine the resulting output sequence on z output.

Graphical user interface

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Q6. Given is the following timing diagram, clock signal, and input waveforms:

1. Derive the state-assigned table.
2. Draw the state diagram.
3. Derive the circuit that implement the FSM.

A screenshot of a computer

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**Graphical user interface

Description automatically generated with low confidence**

**Schematic

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